

**16-Bit Transparent D-Type Latch with 3-State Outputs**

**Features**

- The PI74VCX Family is designed for low voltage operation,  $V_{DD} = 1.8V$  to  $3.6V$
- 3.6V I/O Tolerant Inputs and Outputs
- Supports Live Insertion
- Balanced Drive,  $\pm 24mA$
- Uses patented Noise Reduction Circuitry
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.6V$  at  $V_{DD} = 2.5V, T_A = 25^\circ C$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $< -0.6V$  at  $V_{DD} = 2.5V, T_A = 25^\circ C$
- Power-Off high impedance inputs and outputs
- Industrial operation at  $-40^\circ C$  to  $+85^\circ C$
- Packaging (Pb-free & Green available):  
–48-pin 240-mil wide plastic TSSOP (A)

**Description**

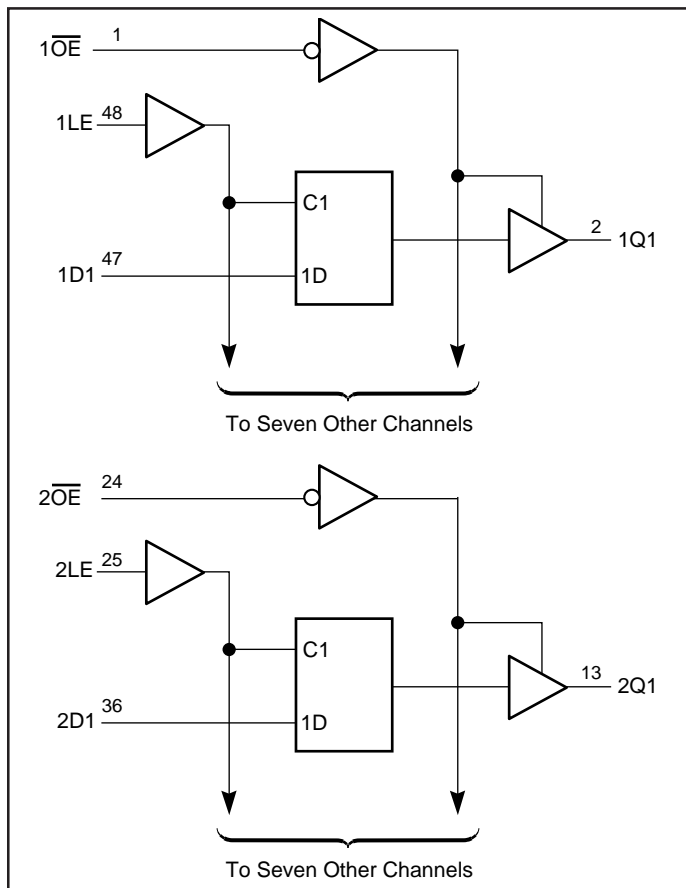
Pericom Semiconductor's PI74VCX16373 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. This device can be used as two 8-bit latches or one 16-bit latch. When the Latch Enable (LE) input is HIGH, the Q outputs follow the (D) inputs. When LE is taken LOW, the Q outputs are latched at the levels set up at the D inputs.

A buffered Output Enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state in which the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.  $\overline{OE}$  does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{DD}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The PI74VCX family is I/O Tolerant, allowing it to operate in mixed 1.8V/3.6V systems.

**Block Diagram**



### Pin Description

Pin Name	Description
$\overline{OE}$	Output Enable Input (Active LOW)
LE	Latch Enable (Active HIGH)
$D_x$	Data Inputs
$Q_x$	3-State Outputs
GND	Ground
VDD	Power

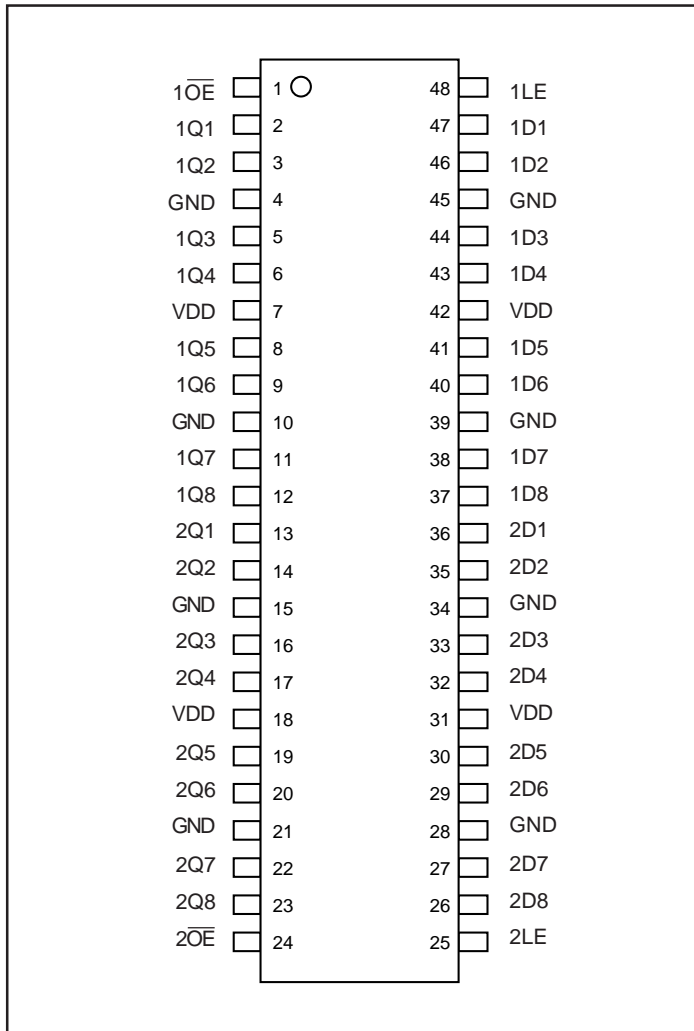
### Truth Table<sup>(1)</sup>

Inputs			Outputs
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q0
H	X	X	Z

#### Notes:

- H = High Signal Level  
 L = Low Signal Level  
 X = Don't Care or Irrelevant  
 Z = High Impedance

### Pin Configuration



## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage Range, $V_{DD}$ .....	-0.5V to 4.6V
Input Voltage Range, $V_I$ .....	-0.5V to 4.6V
Output Voltage Range, $V_O$ (3-States) .....	-0.5V to 4.6V
Output Voltage Range, $V_O^{(1)}$ (Active) .....	-0.5V to $V_{DD} + 0.5V$
DC Input Diode Current ( $I_{IK}$ ) $V_I < 0V$ .....	-50mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O < 0V$ .....	-50mA
$V_O > V_{DD}$ .....	-50mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ ) .....	$\pm 50mA$
DC $V_{DD}$ or GND Current per Supply Pin ( $I_{CC}$ or GND) ....	$\pm 100mA$
Storage Temperature Range, $T_{STG}$ .....	-65°C to 150°C

### Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Notes:

1. Absolute maximum of  $I_O$  must be observed.

## Recommended Operating Conditions<sup>(1)</sup>

Parameters	Description	Conditions	Min.	Max.	Units
$V_{DD}$	Supply voltage	Operating	1.8	3.6	V
		Data Retention Only	1.2	3.6	
$V_{IH}$	High-level input voltage	$V_{DD} = 2.7V$ to 3.6V	2.0		
$V_{IL}$	Low-level input voltage	$V_{DD} = 2.7V$ to 3.6V		0.8	
$V_I$	Input voltage		-0.3	3.6	
$V_O$	Output voltage	Active State	0	$V_{DD}$	
		Off State	0	3.6	
	Output current in $I_{OH}/I_{OL}$	$V_{DD} = 3.0V$ to 3.6V $V_{DD} = 2.3V$ to 2.7V $V_{DD} = 1.8V$		$\pm 24$ $\pm 18$ $\pm 6$	mA
$\Delta t/\Delta v$	Input transition rise or fall rate <sup>(2)</sup>		0	10	ns/V
$T_A$	Operating free-air temperature		-40	85	C

### Notes:

1. Unused control inputs must be held HIGH or LOW to prevent them from floating.
2. As measured between 0.8V and 2.0V,  $V_{DD} = 3.0V$ .

**Electrical Characteristics over Recommended Operating Free-Air Temperature Range**

(unless otherwise noted)

**DC Characteristics (2.7V < V<sub>DD</sub> ≤ 3.6V)**

Parameters	Description	Conditions	V <sub>DD</sub>	Min.	Typ.	Max.	Units
V <sub>IH</sub>	HIGH Level Input Voltage			2.0			V
V <sub>IL</sub>	LOW Level Input Voltage		2.7 - 3.6			0.8	
V <sub>OH</sub>	HIGH Level Output Voltage	I <sub>OH</sub> = -100 μA		V <sub>DD</sub> - 0.2			
		I <sub>OH</sub> = -12 mA	2.7	2.2			
		I <sub>OH</sub> = -18 mA	3.0	2.4			
		I <sub>OH</sub> = -24 mA		2.2			
V <sub>OL</sub>	LOW Level Output Voltage	I <sub>OL</sub> = 100 μA	2.7 - 3.6			0.2	
		I <sub>OL</sub> = 12 mA	2.7			0.4	
		I <sub>OL</sub> = 18 mA	3.0			0.4	
		I <sub>OL</sub> = 24 mA				0.5	
I <sub>I</sub>	Input Leakage Current	V <sub>I</sub> = 0.0V, V <sub>I</sub> = 3.6V	3.6			±5.0	μA
I <sub>OZ</sub>	3-STATE Output Leakage	0 ≤ V <sub>O</sub> ≤ 3.6V V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.7 - 3.6			±10	
I <sub>OFF</sub>	Power-OFF Leakage Current	0 ≤ (V <sub>I</sub> , V <sub>O</sub> ) ≤ 3.6V	0			10	
I <sub>DD</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>DD</sub> to GND	2.7 - 3.6			20	
		V <sub>DD</sub> ≤ (V <sub>I</sub> , V <sub>O</sub> ) ≤ 3.6V				±20	
ΔI <sub>DD</sub>	Increase in I <sub>DD</sub> per input	V <sub>IH</sub> = V <sub>DD</sub> - 0.6V, Other inputs at V <sub>DD</sub> or GND				750	

**DC Characteristics ( $2.3V \leq V_{DD} \leq 2.7V$ )**

Parameters	Description	Conditions	$V_{DD}$	Min.	Typ.	Max.	Units
$V_{IH}$	HIGH Level Input Voltage		2.3 - 2.7	1.6			V
$V_{IL}$	LOW Level Input Voltage					0.7	
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100\mu A$	2.3	$V_{DD} - 0.2$			
		$I_{OH} = -6mA$		2.0			
		$I_{OH} = -12mA$		1.8			
		$I_{OH} = -18mA$		1.7			
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100\mu A$	2.3 - 2.7			0.2	
		$I_{OL} = 12mA$	2.3			0.4	
		$I_{OL} = 18mA$				0.4	
$I_I$	Input Leakage Current	$V_I = 0.0V, V_I = 2.7V$	2.7			$\pm 5.0$	
$I_{OZ}$	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$ $V_I = V_{IH}$ or $V_{IL}$	2.3 - 2.7			$\pm 10$	
$I_{OFF}$	Power-OFF Leakage Current	$0 \leq (V_I, V_O) \leq 3.6V$	0			10	
$I_{DD}$	Quiescent Supply Current	$V_I = V_{DD}$ or GND	2.3 - 2.7			20	
		$V_{DD} \leq (V_I, V_O) \leq 3.6V$				$\pm 20$	

**DC Characteristics ( $1.8V \leq V_{DD} \leq 2.3V$ )**

Parameters	Description	Conditions	$V_{DD}$	Min.	Typ.	Max.	Units		
$V_{IH}$	HIGH Level Input Voltage		1.8 - 2.3	$0.7 \times V_{DD}$			V		
$V_{IL}$	LOW Level Input Voltage					$0.2 \times V_{DD}$			
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100\mu A$	1.8	$V_{DD} - 0.2$					
		$I_{OH} = -6mA$		1.4					
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100\mu A$				0.2			
		$I_{OL} = 6mA$				0.3			
$I_I$	Input Leakage Current	$V_I = 0.0V, V_I = 1.8V$						$\pm 5.0$	$\mu A$
$I_{OZ}$	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$ $V_I = V_{IH}$ or $V_{IL}$						$\pm 10$	
$I_{OFF}$	Power-OFF Leakage Current	$0 \leq (V_I, V_O) \leq 3.6V$		0				10	
$I_{DD}$	Quiescent Supply Current	$V_I = V_{DD}$ or GND		1.8				20	
		$V_{DD} \leq (V_I, V_O) \leq 3.6V$		1.8			$\pm 20$		

**AC Electrical Characteristics<sup>(1)</sup>**

Symbol	Parameters	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, C_L = 30\text{pF}, R_L = 500\Omega$						Units
		$V_{DD} = 3.3\text{V} \pm 0.3\text{V}$		$V_{DD} = 2.5\text{V} \pm 0.2\text{V}$		$V_{DD} = 1.8\text{V}$		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{PLH}, t_{PHL}$	Prop Delay, DTOQ	0.8	3.0	1.0	3.4	1.5	6.0	ns
$t_{PLH}, t_{PHL}$	Prop Delay, LE to Q	0.8	3.0	1.0	3.9	1.5	6.0	
$t_{pZH}, t_{pZL}$	Output Enable Time	0.8	3.5	1.0	4.6	1.5	7.0	
$t_{pHZ}, t_{pLZ}$	Output Disable Time	0.8	3.5	1.0	3.8	1.5	5.0	
$t_{OSHL}, t_{OSLH}$	Output to Output Skew <sup>(2)</sup>		0.5		0.5		0.5	

**Notes:**

- For  $C_L = 50\text{pF}$  add approximately 300ps to AC maximum specification.
- Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH or LOW ( $t_{OSHL}$ ) or LOW to HIGH ( $t_{OSLH}$ ).

**AC Setup Requirements**

Symbol	Parameters	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, C_L = 30\text{pF}, R_L = 500\Omega$						Units
		$V_{DD} = 3.3\text{V} \pm 0.3\text{V}$		$V_{DD} = 2.5\text{V} \pm 0.2\text{V}$		$V_{DD} = 1.8\text{V}$		
		Min.	Typ.	Min.	Typ.	Min.	Typ.	
$t_{SU}$	Setup Time, D to LE	1.5		1.5		2.5		ns
$t_H$	Hold Time, D to LE	1.0		1.0		1.0		
$t_W$	LE Pulse Width, High	1.5		1.5		3.0		

**Dynamic Switching Characteristics**

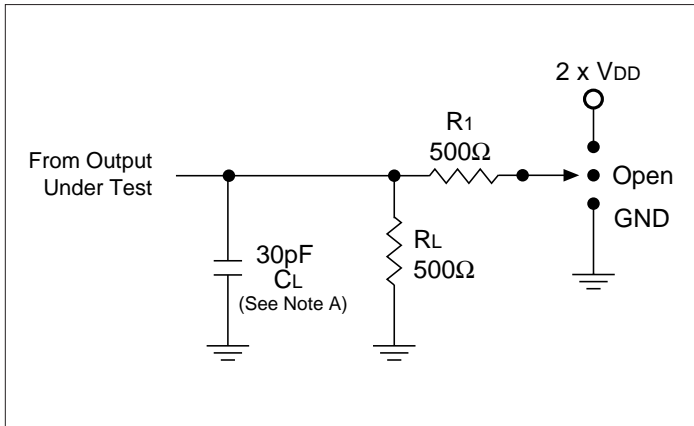
Symbol	Parameters	Conditions	$V_{DD}$	$T_A = +25^{\circ}\text{C}$ Typical	Units
$V_{OLP}$	Quiet Output Dynamic Peak $V_{OL}$	$C_L = 50\text{pF}, V_{IH} = V_{DD}, V_{IL} = 0\text{V}$	1.8	0.25	V
			2.5	0.6	
			3.3	0.8	
$V_{OLP}$	Quiet Output Dynamic Valley $V_{OL}$	$C_L = 50\text{pF}, V_{IH} = V_{DD}, V_{IL} = 0\text{V}$	1.8	-0.25	
			2.5	-0.6	
			3.3	-0.8	
$V_{OLP}$	Quiet Output Dynamic Valley $V_{OH}$	$C_L = 50\text{pF}, V_{IH} = V_{DD}, V_{IL} = 0\text{V}$	1.8	1.5	
			2.5	1.9	
			3.3	2.2	

**Capacitance**

Symbol	Parameters	Conditions	$T_A = +25^{\circ}\text{C}$ Typical	Units
$C_{IN}$	Input Capacitance	$V_{DD} = 1.8, 2.5\text{V or } 3.3\text{V}, V_I = 0\text{V or } V_{DD}$	6	pF
$C_{OUT}$	Output Capacitance	$V_I = 0\text{V or } V_{DD}, V_{DD} = 1.8\text{V}, 2.5\text{V or } 3.3\text{V}$	7	
$C_{PD}$	Power Dissipation Capacitance	$V_I = 0\text{V or } V_{DD}, F = 10\text{ MHz}$ $V_{DD} = 1.8\text{V}, 2.5\text{V or } 3.3\text{V}$	20	

## Test Circuits and Switching Waveforms

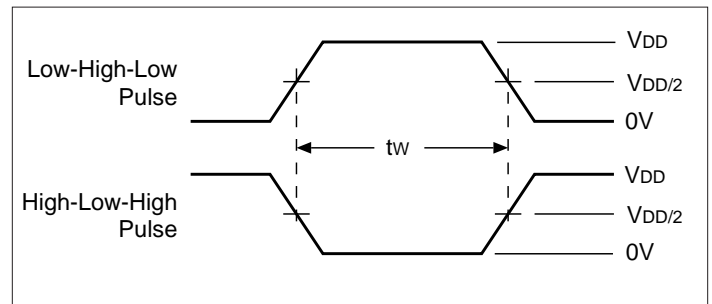
### Parameter Measurement Information ( $V_{DD} = 1.8V - 3.6V$ )



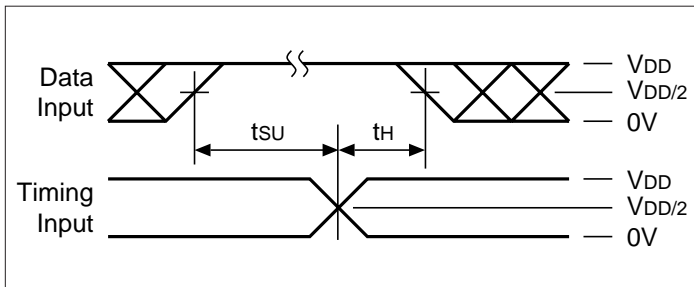
### Switch Position

Test	S1
$t_{PD}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{DD}$
$t_{PHZ}/t_{PZH}$	GND

### Pulse Width



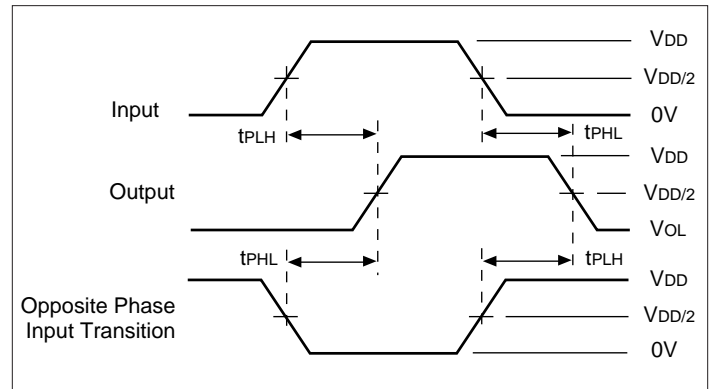
### Setup, Hold, and Release Timing



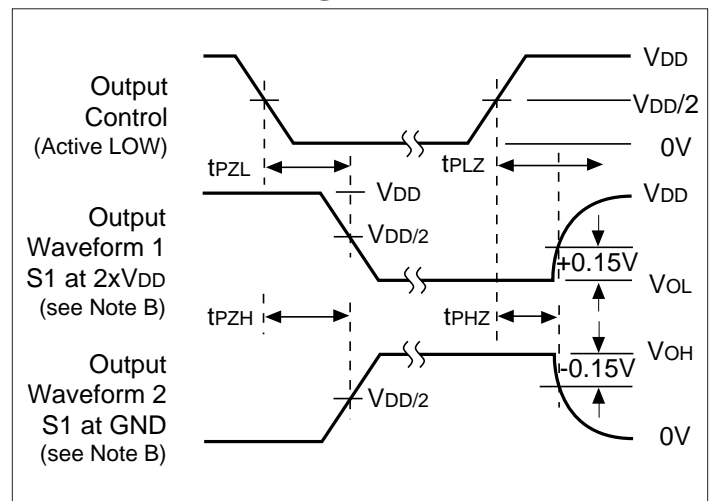
#### Notes:

- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $P_{RR} \leq 10 \text{ MHz}$ ,  $Z_O = 50\Omega$ ,  $t_R \leq 2\text{ns}$ ,  $t_F \leq 2\text{ns}$ , **measured from 10% to 90%, unless otherwise specified.**
- The outputs are measured one at a time with one transition per measurement.

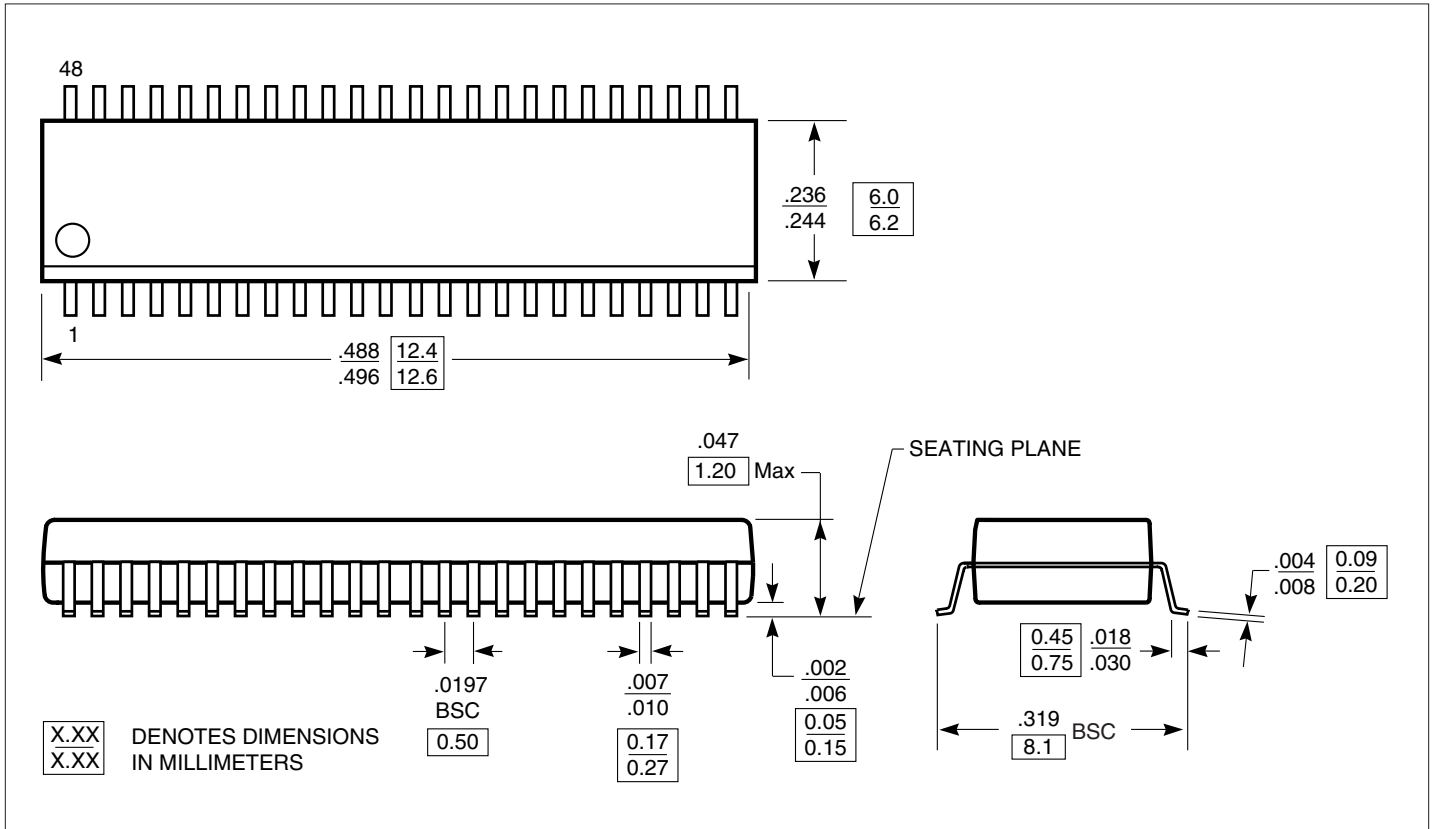
### Propagation Delay



### Enable Disable Timing



### Packaging Mechanical: 48-pin TSSOP (A)



### Ordering Information

Ordering Code	Package Code	Package Type
PI74VCX16373A	A	48-pin TSSOP
PI74VCX16373AE	A	Pb-free & Green, 48-pin TSSOP

#### Notes:

- Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
- E = Pb-free & Green
- Adding an X suffix = Tape/Reel